What is claimed is:

1. A transceiving network controller comprising:

a system bus;

a buffer memory including a transmitting area capable of flexible memory allocation according to transmitted data flow and a receiving area capable of flexible memory allocation according to received data flow, the buffer memory for storing and outputting transmitted data in response to at least one transmitting address signal and for storing and outputting received data in response to at least one receiving address signal;

a flow control unit for generating and outputting threshold control signals for increasing the memory allocation of the transmitting area when a transmission execution signal becomes active and for increasing the memory allocation of the receiving area when a reception execution signal becomes active;

a transmitting controller for generating a plurality of transmitting address signals having a maximum address capable of being changed by the threshold control signals, for outputting at least one transmitting write address signal of the plurality of transmitting address signals with data received from the system bus, and for outputting transmitted data output from the buffer memory to a lower layer, the transmitted data being output from the buffer memory in response to at least one transmitting read address signal of the plurality transmitting address signals, and in response to the transmission execution signal becoming active upon receipt of the data received from the system bus; and

a receiving controller for generating a plurality of receiving address signals having a maximum address capable of being changed by the threshold control signals, for outputting at least one receiving write address signal of the plurality of receiving address signals with data received from the lower layer, and for outputting received data output from the buffer memory to the system bus, the received data being output from the buffer memory in response to at least one receiving read address signal of the plurality of receiving address signals, and in response to the reception execution signal becoming active upon receipt of the data received from the lower layer.

2. The transceiving network controller of claim 1, wherein the flow

control unit generates a threshold control signal for maintaining the memory allocation of the transmitting area and the receiving area when the transmission execution signal and the reception execution signal become active simultaneously.

3. The transceiving network controller of claim 1, wherein the flow control unit generates a threshold control signal for equalizing the memory allocation of the transmitting area and the receiving area.

4. The transceiving network controller of claim 1, wherein the flow control unit generates a threshold control signal for maintaining the memory allocation of the transmitting area and the receiving area at a predetermined threshold in accordance with a predetermined setting.

5. The transceiving network controller of claim 1, wherein the transmitted data and the received data are transmitted using a full duplex method.

6. The transceiving network controller of claim 1, wherein the transmitted data and the received data are transmitted using a half duplex method.

7. A method for controlling buffer memory allocation and data flow, the buffer memory including a transmitting area and a receiving area capable of flexible memory allocation according to transmitted data flow and received data flow, respectively, the method comprising:

storing and outputting transmitted data in and from the buffer memory in response to at least one transmitting address signal;

storing and outputting received data in and from the buffer memory in response to at least one receiving address signal;

generating and outputting threshold control signals for increasing memory allocation of the transmitting area when a transmission execution signal becomes active and for increasing memory allocation of the receiving area when a reception execution signal becomes active;

generating a plurality of transmitting address signals having a maximum address capable of being changed by the threshold control signals;

outputting at least one transmitting write address signal of the plurality of transmitting address signals with data received from a system bus;

outputting transmitted data output from the buffer memory to a lower layer, the transmitted data being output from the buffer memory in response to at least one transmitting read address signal of the plurality of transmitting address signals, and in response to the transmission execution signal becoming active state upon receipt of the data received from the system bus;

generating a plurality of receiving address signals having a maximum address capable of being changed by the threshold control signals;

outputting at least one receiving write address signal of the plurality of receiving address signals with data received from the lower layer; and

outputting received data output from the buffer memory to the system bus, the received data being output from the buffer memory in response to at least one receiving read address signal of the plurality of receiving address signals, and in response to the reception execution signal becoming active upon receipt of the data received from the lower layer.

8. The method of claim 7, wherein the threshold control signals maintain the memory allocation of the transmitting area and the receiving area when the transmission execution signal and the reception execution signal become active simultaneously.

9. The method of claim 7, wherein the threshold control signals equalize the memory allocation of the transmitting area and the receiving area when power is turned on.

10. The method of claim 7, wherein the threshold control signals maintain the memory allocation of the transmitting area and the receiving area at a predetermined threshold in accordance with a predetermined setting.

11. The method of claim 7, wherein the transmitted data and the received data are transmitted using a full duplex method.

12. The method of claim 7, wherein the transmitted data and the received data are transmitted using a half duplex method.

13. A transceiving network controller comprising:

a system bus;

a buffer memory including a transmitting area capable of flexible memory allocation according to transmitted data flow and a receiving area capable of flexible memory allocation according to received data flow, the buffer memory for storing and outputting transmitted data in response to at least one transmitting address signal and for storing and outputting received data in response to at least one receiving address signal;

a flow control unit for generating and outputting threshold control signals for increasing the memory allocation of the transmitting area when a transmission execution signal becomes active and for increasing the memory allocation of the receiving area when a reception execution signal becomes active;

a transmitting controller for generating a plurality of transmitting address signals; and

a receiving controller for generating a plurality of receiving address signals.

14. The transceiving network controller of claim 13, wherein each of the plurality of transmitting address signals includes a maximum address capable of being changed by the threshold control signals.

15. The transceiving network controller of claim 13, wherein each of the plurality of receiving address signals includes a maximum address capable of being changed by the threshold control signals.

16. The transceiving network controller of claim 13, wherein the transmission execution signal becomes active when the transmitting controller receives transmitted data from the system bus.

17. The transceiving network controller of claim 13, wherein the reception execution signal becomes active when the receiving controller receives received data from a lower layer.

18. A method for controlling buffer memory allocation and data flow, the buffer memory including a transmitting area and a receiving area capable of flexible memory allocation, the method comprising:

storing and outputting transmitted data in and from the buffer memory in response to at least one transmitting address signal;

storing and outputting received data in and from the buffer memory in response to at least one receiving address signal;

generating and outputting threshold control signals for increasing memory allocation of the transmitting area when a transmission execution signal becomes active and for increasing memory allocation of the receiving area when a reception execution signal becomes active;

generating a plurality of transmitting address signals having a maximum address capable of being changed by the threshold control signals; and

generating a plurality of receiving address signals having a maximum address capable of being changed by the threshold control signals.